Master internship position

DACLE
DCOS

Laboratoire
d'électronique
et de technologie

Field:

Chemistry for nanos	☐	Molecular electronics	☐	Process Technologies	☒
Imaging devices & Systems	☐	Nanocharacterization	☐	RF Devices & Systems	☐
Materials	☐	Nanoelectronics	☐	Spintronics	☐
Memory technologies	☐	Nanos for Energy	☐	Other	☒
MEMS and sensors	☐	Nanoscale simulation	☒	Design layout and SPICE simulation	
Microtechnologies for bio	☐	Photonics	☐		

Required	Duration	Start		
ongoing MSc	6 months	Q1 2017		

Topic: Design / Technology Co-Optimization of standard cells for monolithic 3D CMOS technology exploiting a high back-bias capability

Context:

Fully-Depleted-Silicon-On-Insulator (FDSOI) CMOS architectures are now in production at the 28nm and 22nm technology nodes by STMicrolectronics and Global Foundries [http://www.soiconsortium.org/fully-depleted-soi/presentations/SOI-Consortium-FD-SOI-Symposium-Sanjose-2016]. The great advantage of this technology, compared to the finFETs alternative, is the back-bias efficiency, i.e. the capability to play with an extra gate electrode (underneath the device), in order to tune the electrical characteristics. This enables saving dynamic power and thus for this technology to be highly competitive, especially for low-cost low-power Internet-of-Things (IoT) applications, which should be the growing market of the next decade.

In order to leverage even more the back-bias capability for the next nodes, solutions exist for planar integration [L. Grenouillet et al, IEDM'12]. But even more opportunities can be provided by a 3-dimensional (3D) integration.

LETI is a pioneer in the monolithic 3D CMOS integration (see Fig.1 and [P. Batude et al., VLSI'15]). We have been developing technology and design kits (including spice model, parasitics extraction tools and design library) in order to assess, enable and benchmark this architecture not only for More-Moore but also for More-than-Moore roadmaps.

The purpose of this MSc internship is to study the interest of the LETI 3D monolithic technology, namely CoolCube™, in improving the back bias capability of the planar FDSOI technology. Especially, the student will analyze, whether CoolCube™ can extend a CMOS 14nm LETI planar FDSOI digital library with some specific Ultra-Low-Power 3D cells, with no or limited area penalty.

This study is in-between CMOS technology and design.

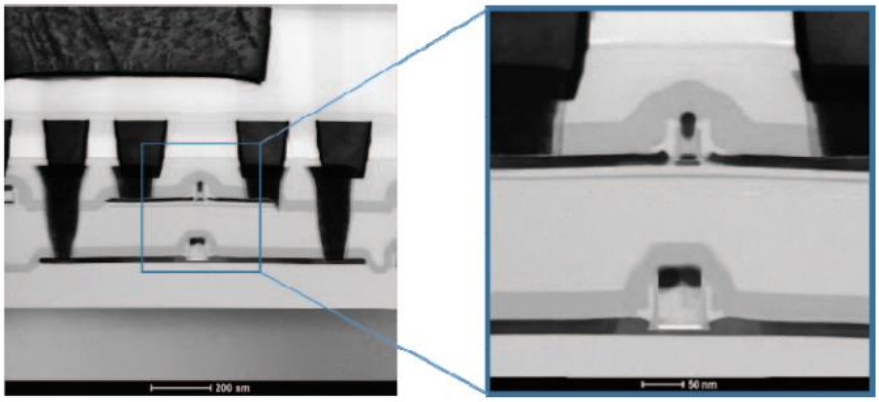

Figure 1: Transmission Electron Microscopy image of CMOS Coolcube integration performed at LETI [L. Brunet et al., VLSI'16].

Keywords: 3D, standard cell layout, design / technology co-optimization (DTCO), CMOS device and integration, nanotechnology

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Study:

The content of the internship will cover the following sections:

- Bibliography on FDSOI, CMOS device and integration, digital library, back bias techniques
- Technology of 3D contact: state-of-the-art in the literature, discussion with process engineer and CMOS integration team in order to define a targeted process integration for this study
- Standard cell layout using Virtuoso and performance simulation using a spice model and a dedicated parasitics extraction tool for different cells, geometries and circuit environment (load, supply voltages...). Break-out of the capacitance components impacting the cell performance. Co-optimization of the design geometries and targeted process integration flow in order to be competitive in terms of performance / power and area on dedicated cells. Designs will be performed for both 3D and 2D cells, as a reference.

Such a co-optimization, i.e. a continuous feedback between design and technology through silicon validation is crucial and required for advanced CMOS technologies.

Lab

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